REMARKS

Claims 1-10 are pending in the present Application.

Drawings

The Examiner objected the drawings. In FIG. 1 the Examiner objected the labeling "Vhigh" and "Vlow". The Examiner suggested the labeling V_{high} and V_{low}.

In response, Applicant introduced the suggested labeling in amended FIG. 1.

In FIG. 9, the Examiner objected the labeling "E[DB]". Instead the Examiner suggested "E[dB]".

In response, Applicant introduced the suggested labeling.

Specification

The Examiner objected the labeling scheme of the specification, in particular that indices should be shown as subscripts, not in-line characters.

In response, Applicant amended the specification to show indices as subscripts.

The Examiner objected paragraph [0041] for not reciting the number of resistors in accordance with the corresponding figures.

In response, Applicant amended paragraph [0041] to be consistent with the corresponding figures.

Claim Objections

Claims 1-6 are objected to because of the following informalities:

"As per claim 1, the recitation in line 1 of claim 1 comprising' is improper (see claims 7 and 8); it is suggested to be changed to 'comprising'."

In response, Applicant amended the claim to read "comprising:".

Claims 2-6 are objected because they depend directly or indirectly from claim 1 and claim 1 is objected.

In response, Applicant points out that amended claim 1 does not have the above informality anymore and thus the objection is overcome.

Claim Rejections - 35 USC § 112

Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states:

> "As per claim 8, claim 8 is rejected because claim 8 recites the limitation "every cycle of the counter" at the beginning of line 4. There is insufficient antecedent basis for this limitation in the claim."

In response, Applicant respectfully traverses the rejection and points out that, for example, in [0032] the amended specification describes an embodiment corresponding to this claim limitation:

> "That is, the output (Q_1-Q_{1n}, QB_1-QB_n) of each flip-flop (FF_1-FF_n) reverses at every cycle of the signals (CL~~C~~K and Q_1-Q_{n-1}) inputted to the flip-flop (FF_1-FF_n)."

Claims 9-10 are rejected because they depend from claim 8.

In response, Applicant points out that claim 8 is now fully supported by the specification, and thus claims 9 and 10 are also supported.

Claim Rejections - 35 USC § 103

Claims 1, 5, 6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan (US 6249876 B1) in view of Greiss (US 5731728 A). The Examiner states:

> "As per claim 1, Balakrishnan discloses an electromagnetic interference cancellation system comprising a control signal generation unit having a counter that counts n-bit signals to output a first output signal of n bits with a count value (figure 1 block 140 column 4 lines 28-39); a voltage control unit that outputs a voltage having a step index level corresponding to the count value of the control signal (figure 1 block 150 column 4 lines 28-39); and an oscillator that generates a clock signal having a frequency corresponding to the voltage outputted from the voltage control unit (figure 1 block 110 column 4 lines 28-39). Balakrishnan doesn't disclose a second output signal having a level that is opposite to the first output signal the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter. Greiss discloses a second output signal having a level that is opposite to the first output signal the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter (figure 3 column 3 lines 10-22). Balakrishnan and Greiss are analogous art because they are from the same field of electromagnetic interference reduction. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Balakrishnan the algorithm disclosed by Greiss. The suggestion/motivation for doing so would have been to reduced EMI spectral density of the clock signal (Greiss abstract).

Applicant respectfully traverses the rejection in light of the following remarks.

1. Balakrishnan does not have a "*voltage* control unit that outputs a *voltage*"

Claim 1 requires, in pertinent part:

"a *voltage* control unit that outputs a *voltage*..." (emphasis added)

The Examiner identified Balakrishnan's "block 150" as the claimed voltage control unit. This is incorrect. First, Balakrishnan's block 150 is a current source, as evidenced even by its name: it is called "frequency jittering *current* source 150" (col. 4, l.36).

Second, the entire operation of D/A converter 150 and its connection to oscillator 120 is given in terms of currents, not voltages (col. 5, l. 5-21): The "jittering *current* source 150" includes "jittering *current* sources" 152, 156, 160, 164, which provide a fraction of the *current*: I/200, I/100, I/50, and I/25. Then (col. 5, l. 24-28):

> "the largest current source 164 may *supply* no more than 10% *of the current I* provided by the primary current source 122. The drain of transistors 154, 158, 162 and 166 are joined together such that the supplemental frequency jittering *current* sources of the D-to-A converter 150 can be provided to supplement the primary *current* source 122." (emphasis added)

In sum, Balakrishnan's block 150 is a current source, not a voltage control unit, which supplies a current, not a voltage.

2. Neither Greiss nor Balakrishnan has a control unit, which "*alternately* outputs the first and second output signals"

Claim 1 requires, in pertinent part:

> "a second output signal having a level that is opposite to the first output signal, the control signal generation unit *alternately outputs the first and second output signals* as control signals according to a cycle of the counter" (emphasis added)

Balakrishnan does not have a second output, as admitted by the Examiner. Therefore, Balakrishnan cannot output the first and second signals alternately.

In Greiss, the Examiner identified inverter 308 as the second output generation unit. Therefore, Greiss' first signal is 304 and the putative second signal is 312.

However, Greiss does not output these two signals "alternately". Greiss outputs the signals 304 and 312 in parallel, continuously. This is clear from his overall layout: block 308 is a simple inverter, which inverts 304 and continuously outputs it. Both original signal 304 and inverted signal 312 are continuously received by block 306.

The Examiner referred to column 3 lines 10-22 in Greiss as support for his assertion. Tellingly, the referenced passage does not describe outputting signals *alternately* anywhere.

Therefore, neither Balakrishnan, nor Greiss outputs the first and second signal *alternately*.

3. Neither Greiss nor Balakrishnan has "a second output signal having a level that is *opposite* to the first output signal"

Claim 1 requires, in pertinent part:

> "a second output signal having a level that is *opposite* to the first output signal, the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter" (emphasis added)

Balakrishnan does not have a second output, as stated by the Examiner. Therefore, Balakrishnan cannot output the second signals that is opposite to the first signal.

In Greiss' circuit the putative second signal is not opposite either, because it is *delayed* by a half clock cycle (col. 3, l. 17-20):

> "The invert circuit 308 inverts the input clock signal 302 *by about one half clock cycle* ("about", since the invert circuit 308 also has a *delay effect* on the input clock signal 302) and provides the resultant *inverted delayed clock signa*l 310 (FIG. 4B) to a second input *312* of the digital modulator 306." (emphasis added)

The delay is substantial, it is one half of a cycle. Therefore, this delayed signal 312 is not *opposite* to the first clock signal 304.

4. There is no motivation to combine Balakrishnan with Greiss: Balakrishnan already has the feature Greiss may have promised

Claim 1 requires, in pertinent part:

> "a second output signal having a level that is opposite to the first output signal, the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter"

The Examiner stated that Balakrishnan does not have this claim element, but Greiss does, and thus Balakrishnan in view of Greiss obviates claim 1.

In response, Applicant points out that Balakrishan's FIG. 2 may suggest that his oscillator frequency increases and then drops sharply. This may be interpreted that a second output signal is needed to create a system where the frequency increases and then decreases gradually. Such a system may be provided by Greiss.

However, Balakrishnan's FIG. 5 illustrates that his system in fact *does* produce an oscillator output signal whose frequency increases and then decreases gradually in time. Therefore, there is no motivation to introduce Greiss' circuitry into Balakrishnan's system, since Greiss, at best, promises a feature which is already present in Balakrishnan.

5. There is no motivation to combine Balakrishnan with Greiss: the two technologies are incompatible and alien

Greiss' technique is qualitatively different from Balakrishnan's. Balakrishnan smoothly varies the frequency, as seen in his FIG. 5.

In contrast, Greiss does not vary the frequency of his clock. Greiss decimates the clock signal. As shown e.g. in his FIGs. 2 and 4, Greiss "removes one transition" (abstract). Therefore, *Greiss' clock retains its operating frequency and remains synchronous with the original clock.* At most, the decimation results in a phase shifted clock signal.

The difference of the techniques can be appreciated by comparing Balakrishnan's FIG. 5, with its varying frequency, to Greiss' FIGs. 2 and 4, which show a constant frequency, with occasional transitions missing.

Greiss himself explains that retaining an operation synchronous with the clock is a key feature (abstract):

"Significantly, the modulated clock signal is synchronous with the first clock".

Combining Greiss system with Balakrishnan's would have ruined this synchronous operation. Therefore, the two techniques are qualitatively different, and thus a person of ordinary skill would not have been motivated to import Greiss's technology into Balakrishnan.

6. The techniques of Balakrishnan and Greiss are substantially different, as also demonstrated by the lack of a correspondence of circuit elements

Claim 1 requires, in pertinent part:

> "a second output signal having a level that is opposite to the first output signal, the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter"

The Examiner stated that Greiss discloses the above claim limitation. However, tellingly, the Examiner did not identify the individual claim elements in Greiss.

There is a good reason for that. Greiss does not have many of the required claim elements.

- Greiss does not have a "counter", he only has an oscillator.

- Therefore, Greiss does not have (he cannot have) a "cycle of the counter" either.

- Greiss does not have an n-bit signal: he has a periodic clock signal.

- Greiss does not output the two signals "according to a cycle of the counter": it outputs them in parallel.

Because of this extensive list of missing claim elements, it is far from obvious how a person of ordinary skill in the art would combine Balakrishnan's system with that of Greiss.

At least for the above reasons 1-6, Balakrishnan, alone or in view of Greiss, does not obviate independent claim 1.

Dependent claims 5 and 6 depend from independent claim 1, which was shown to be allowable. Therefore, dependent claims 5 and 6 are allowable themselves, at least for this reason.

Independent claim 8 is allowable for analogous reasons 1-6 as claim 1. Dependent claims 9 and 10 are allowable as claim 8 was shown to be allowable.

Allowable Subject Matter

Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response, Applicant gratefully thanks the Examiner for recognizing the allowability of claims 2-4 if rewritten in independent form. However, since independent claim 1 was shown to be allowable, claims 2-4 are allowable without rewriting in independent form.

Claim 7 is allowed.

In response, Applicant gratefully thanks the Examiner for allowing claims 7.

CONCLUSION

In light of the above remarks, Applicant respectfully submits that all pending claims are in condition of allowance and therefore their allowance is requested. If any of the claims require further clarification or discussion, the undersigned is readily available at (415) 772-7434.

Certificate of Mailing

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Annotated Sheet

FIG.1

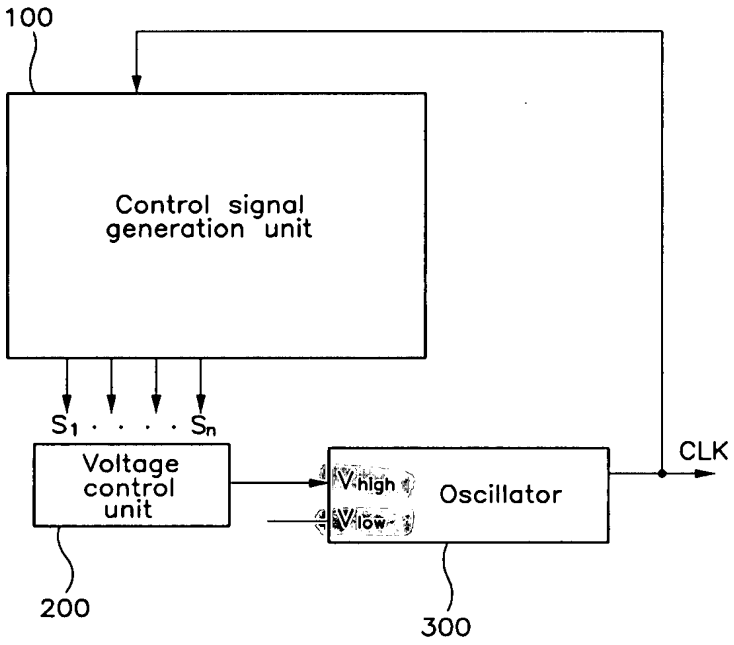

FIG.9